RC7316

Three-State ATE Pin Electronics Driver

Features

- High output slew rate (3.2 V/ns) typical driving coax
- Wide output voltage range (-2.0V to +7V), and up to 9 Vp-p swings
- Three-state/high impedance output
- High repetition rate (550 MHz for ECL swings)
- Low output offset (40 mV typical) and output offset drift (0.1 mV/°C typical
- Low leakage (10 nA typical) and low output capacitance (3.0 pF typical) in high impedance inhibit mode
- 100 mA typical dynamic current drive capability
- High speed differential inputs with wide common mode range for ease of interface to ECL as well as TTL and CMOS levels
- Output short circuit protection (Safe Operating Area protection with current limiting and thermal shutdown)
- Available in 16 Lead Hybrid Flatpack
- RC7316TEL is pin-for-pin compatible with AD1321, AD1322, and AD1324

Applications

- ATE pin electronics driver
- Precision waveform generator
- Level translator
- Differential line receiver
- General purpose driver
- Laser driver
- CRT preamplifier

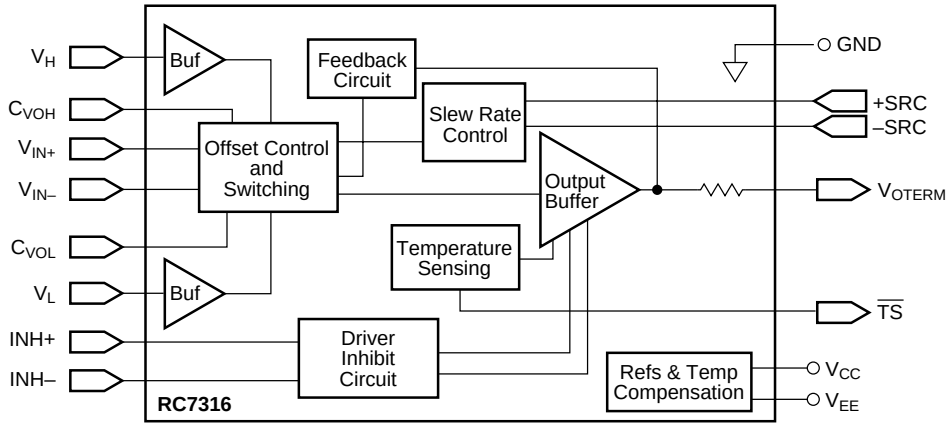
Description

The RC7316 Pin Electronics Driver is designed for use in ultra high speed ATE systems which require pin drivers with three state capability and high slew rates. The RC7316 has the ability to drive a 50Ω transmission line of up to 2 feet in length with a slew rate of 3.2 V/ns and repetition rate of over 550 MHz for ECL output levels. These features, combined with a maximum output swing of 9.5 Vp-p over the range of -3.0V to +7V, provide this circuit with the ability to test TTL, CMOS, ECL and GaAs devices. The high and low limits of the output swing are set through the program pins V_H and V_L, respectively. The transfer characteristic from the program pins to the output pin is unity gain with very low offset drift. The V_H and V_L inputs have been buffered to operate with low bias currents (1 μA typical) allowing direct coupling to the output of a DAC.

When the RC7316 is used on an I/O pin, it may be forced into the high impedance state through the INH+ and INH- differential inputs. In the high impedance state, excellent isolation is provided between the output of the disabled driver and the pin by virtue of low driver output capacitance (3.0 pF typical) and low output leakage (10 nA typical).

The RC7316 is provided with high speed differential ECL inputs for ease of interface with the differential ECL outputs of a timing generator. The inputs have a voltage range of -2V to +6V, so that if required, an input may be driven by TTL or CMOS devices provided that the other input is fed to the appropriate threshold value.

Block Diagram



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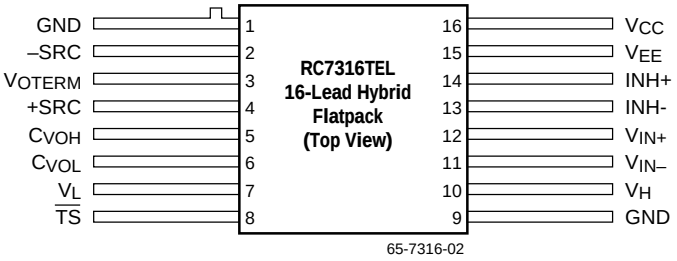
Description (continued)

The pin driver is available in 50Ω series terminated RC7316 (TEL) configurations. The RC7316TEL is pin-for-pin compatible with Analog Devices' AD1321, AD1322 and AD1324 drivers.

The RC7316 is implemented using Fairchild Semiconductor's high frequency BiCMOS process.

Pin Assignments



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Pin Descriptions

Pin Name	Pin Number	Pin Function Description
C_{VOL}, C_{VOH}	6, 5	Bypass capacitor for V_{OH} and V_{OL} respectively. Pins C_{VOL} and C_{VOH} should be bypassed to the ground plane with a 1,000 pF chip capacitor placed as close to the pin as possible.
GND	1, 9	Chip ground. Should be connected to the printed circuit board's ground plane at the pin.
INH+, INH-	13, 14	Differential digital inputs. When INH is true (i.e. INH+ > INH-) the driver is forced into the high impedance state. Although these inputs are normally driven by ECL signals, they have a wide enough common mode range that any one of the inputs may be driven by a TTL or CMOS signal provided that the other input is tied to the appropriate threshold voltage.
+SRC	4	Slew rate control for the positive edge. Slew rate of the positive edge changes as the control voltage is changed from -2.0V to +2.0V. +SRC can also be programmed with a current DAC or set to a fixed value using a resistor. Optionally, pin 4 can be NC. (No Connection)
–SRC	2	Slew Rate Control for the negative edge. Slew rate of the negative edge changes as the control voltage is changed from -2.0V to +2.0V. -SRC can also be programmed with a current DAC or set to a fixed value using a resistor. Optionally, pin 2 can be NC. (No Connection)
$\overline{TS}$	8	Active low output notifies thermal shutdown has occurred. In the event of a short circuit or other fault that causes the die temperature to become excessively large, the thermal shutdown will kick in at a die temperature between 115°C and 160°C. If the fault persists, the device will toggle back and forth between shutdown and normal operation at a frequency in the tens of Hertz. TS is an open collector output capable of driving two standard TTL loads. The TS pins of several drivers may be wire-ORed together and input to a latch to indicate an alarm condition. Optionally, pin 8 can be NC.
V_{CC}	16	Quiet positive supply. The nominal value is 10V ±3%. For output high voltage levels (V_{OH}) greater than the nominal value of +7V, V_{CC} should be raised 3V above the maximum value of V_{OH}. Whenever V_{EE} is lowered to provide margin at the output low level, V_{CC} should also be lowered by the same amount. V_{CC} should be bypassed to ground with a 10,000 pF chip capacitor placed as close to the pins as possible.

Pin Descriptions (continued)

Pin Name	Pin Number	Pin Function Description
V_{CCO}		Positive supply for the RC7316 output stage. This supply is brought out separately to minimize the supply noise generated when the output switches. V_{CCO} should be bypassed to the ground plane with a 10,000 pF chip capacitor placed as close to the pin as possible and then immediately connected to V_{CC}.
V_{EE}	15	Quiet negative supply. The nominal value is -5.2V ±5%. For output low voltage levels (V_{OL}) less than the nominal value of -2.5V, V_{EE} should be lowered 3V below the minimum value of V_{OL}. Whenever V_{CC} is raised to provide margin at the output high level, V_{EE} should also be raised by the same amount. V_{EE} should be bypassed to ground with a 10,000 pF chip capacitor placed as close to the pins as possible.
V_{EEO}		Negative supply for the RC7316 output stage. This supply is brought out separately to minimize the supply noise generated when the output switches. V_{EEO} should be bypassed to the ground plane with a 10,000 pF chip capacitor placed as close to the pin as possible and then immediately connected to V_{EE}.
V_H	10	Analog program input that sets the output high level (V_{OH}) The transfer characteristic from V_H to V_{OH} is nominally unity gain.
V_{IN+}, V_{IN-}	11,12	Differential digital inputs. The output will toggle between the two levels dictated by V_H and V_L as the differential signal is switched. Although these inputs are normally driven by ECL signals, they have a wide enough common mode range that any one of the inputs may be driven by a TTL or CMOS signal provided that the other input is tied to the appropriate threshold voltage.
V_L	7	Analog program input that sets the output low level (V_{OL}). The transfer characteristic from $V_L$to V_{OL} is nominally unity gain.
V_O		Driver output on RC7316. The output impedance is 10Ω ±2Ω. The output is usually back terminated in the characteristic impedance of the transmission line it drives. For a 50Ω line, a 40Ω ±1% resistor should be placed externally as close to the output pin as possible to minimize reflections and ringing. The resistor should also be able to dissipate 0.8Ω to sustain the short circuit current of the output.

Absolute Maximum Ratings[1]

Parameter	Min.	Max.	Units
Positive power supply, V_{CC}		13	V
Negative power supply, V_{EE}	-8.2		V
Difference between V_{CC} and V_{EE}		16	V
Input voltage at V_{IN+}, V_{IN-}, INH+, INH-	V_{CC}-12	V_{EE}+12	V
Input Voltage at V_H, V_L	V_{CC}-13	V_{EE}+13	V
Differential input voltage, $\lvert V_{IN+} - V_{IN-} \rvert$, $\lvert V_{INH+} - V_{INH-} \rvert$		6	V
Difference between V_H & V_L ($\lvert V_H - V_L \rvert$)		11	V
Input voltage at +SRC, -SRC	-3	+7	V
Slew rate control current	-2.0		mA
Driver Output Voltage	V_{CC}-13	V_{EE}+13	V
Output voltage at TS		5	V
Duration of short-circuit to ground		Indefinite	
Operating temperature range	0	70	°C
Storage temperature range	-65	+125	°C
Lead temperature range (Soldering 10 seconds)		300	°C

Notes:

1. “Absolute maximum ratings” are those beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. If the device is subjected to the limits in the absolute maximum ratings for extended periods, its reliability may be impaired. The tables of Electrical Characteristics provide conditions for actual device operation.

Recommended Operating Conditions

Symbol	Parameters	Min.	Typ.	Max.	Units
T_C	Case operating temperature	0	25	+70	°C
V_{CC}	Positive supply voltage	9.7	10.0	10.3	°C
V_{EE}	Negative supply voltage	-5.45	-5.2	-4.95	V
V_{CC}-V_{EE}	Difference between positive and negative supply		15.2	15.8	V
V_{OH}, V_{OL}	Range for output high level and output low level	-3.0		7.0	V
V_{OH}-V_{OL}	Output amplitude	0.1		9.5	V
R_T	Output back-termination resistor		41		

DC Electrical Characteristics

V_{CC} = 10V ±3%, V_{EE} = -5.2V ±5%, T_A = 25°C (flow ≥ 300 Lfm) and the load is a 50Ω transmission line with 2.0 ns one-way delay, unless otherwise specified. The transmission line is back-terminated in 50Ω (±5%) using an external resistor (RC7316).

Symbol	Parameters	Test Conditions	Min.	Typ.	Max.	Units
Diffential Inputs V_{IN+}, V_{IN-}, V_{INH+}, V_{INH-}						
V_{IN+}, V_{IN-}	Absolute Voltage @ Data Inputs		-2.0		+6.0	V
V_{INH+}	Absolute Voltage @ Inhibit					
V_{INH-}	Inputs INH+, INH-		-2.0		+5.0	V
V_{ID}	Differential Input Range	$\lvert V_{IN+} - V_{IN-} \rvert$	0.4	ECL	5.0	V
V_{DINH}	Differential Inhibit Input Range	$\lvert V_{INH+} - V_{INH} \rvert$	0.4	ECL	5.0	V
I_{IN+}, I_{IN-}	Input Bias Current @ Data Inputs	-2V ≤ V_{IN+}, V_{IN-} ≤ +6V	-100	-35		µA
I_{INH+}, I_{INH-}	Input Bias Current @ Inhibit Inputs	-2V ≤ V_{INH+}, V_{INH-} ≤ +5V	-150	-50		µA
Voltage Program Inputs V_H, V_L						
V_H	V_H Range	V_{CC} = 10V; V_{EE} = -5.2V	-2.0		+7.0	V
		V_{CC} = 12V; V_{EE} = -3.2V	0		+9.0	V
		V_{CC} = 8V; V_{EE} = -7.2V	-4.0		+5.0	V
V_L	V_L Range	V_{CC} = 10V; V_{EE} = -5.2V	-2.0		+6.0	V
		V_{CC} = 12V; V_{EE} = -3.2V	0		+8.0	V
		V_{CC} = 8V; V_{EE} = -7.2V	-4.0		+4.0	V
I_H	Bias Current @ V_H	-1V ≤ V_H ≤ +7V; V_L = -3.0V		1.0	5.0	µA
I_L	Bias Current @ V_L	-3V ≤ V_L ≤ +5V; V_H = 6.0V	-5.0	-1.0		µA
TCI_H	Temperature Drift in I_H	V_H = 7.0V; 25°C ≤ T_C ≤ 70°C output not switching			0.1	µA/°C
TCI_L	Temperature Drift in I_L	V_L= -3.0V; 25°C ≤ T_C ≤ 70°C output not switching			0.1	µA/°C
ΔIBDC	Variation in I_H, $I_L$with power supply and DC voltage at V_H or V_L	-1V ≤ V_H ≤ +7V -2V ≤ V_L ≤ + 6V	-1		1	µA
$V_{H,L}$BW	-3 dB bandwidth from V_H or V_L to the output	-1V ≤ V_H ≤ +7V; -2V ≤ V_L ≤ +6V; V_H-V_L= 2.0V			50	kHz
Signal Output V_O, V_{OTERM}						
V_O	Output Voltage Range	V_{CC} = 10V; V_{EE} = -5.2V	-2.0		+7.0	V
		V_{CC} = 12V; V_{EE} = -3.2V	0		+9.0	V
		V_{CC} = 8V; V_{EE} = -7.2V	-4.0		+5.0	V
V_A	Amplitude	$\lvert V_{OH} - V_{OL} \rvert$	0.1		9.5	V
δV_{OH}	Offset to Output High Level	-1V ≤ V_H ≤ +6V; V_L = -2V	-100	-40	100	mV
		$\delta V_{OH} = \lvert V_H - V_{OH} \rvert$				
δV_{OL}	Offset to Output Low Level	-2V ≤ V_L ≤ +6V; V_H = +7V	-100	-40	100	mV
		$\delta V_{OL} = \lvert V_L - V_{OL} \rvert$				
VTC	Output Voltage Drift	-1V ≤ V_{OH} ≤ +7V		0.1		mV/°C
ε_G	Gain Error	-2V ≤ V_{OL} ≤ +7V	-1.0	±0.5	+1.0	%V_{SET}
ε_L	Linearity Error	0V ≤ V_{OUTPUT} ≤ +5V	-0.5	±0.2	+0.5	%V_{SET}
		-2V≤ V_{OUTPUT} ≤ +7V	-1.0	±0.6	+1.0	%V_{SET}
Z_{OUT}	Output Impedance			50		

DC Electrical Characteristics (continued)

Symbol	Parameters	Test Conditions	Min.	Typ.	Max.	Units
I_{ZL}	Output Leakage Current in Inhibit Mode	$-2.0V \le V_O \le +6.5V$	-200	±10	+200	nA
I_{DC}	DC Current Drive		50			mA
I_{AC}	AC Current Drive		70	100		mA
Thermal Shutdown Output (TS) (Open Collector Output)						
I_{CL}	DC Current Limit		70	110	130	mA
V_{OL}	Output Low Level	I_{OL} = 4 mA			0.5	V
T_{TS}	Shutdown Die Temperature		115	135	160	°C
Other						
V_S	Rail to Rail Supply Voltage	$V_{CC} - V_{EE}$			17	V
V_{CC}	Positive Supply		+8.0	+10.0	+12.0	V
V_{EE}	Negative Supply		-7.2	-5.2	-3.2	V
I_{CC}	Positive Supply Current			85		mA
I_{EE}	Negative Supply Current			95		mA
$PSRV_O$	Output Level Power Supply	V_{CC}; ΔV_{CC} = ±2.5%		40		dB
	Rejection Ratio	V_{EE}; ΔV_{EE} = ±2.5%		40		dB
$PSRV_{SL}$	Output Slew Rate Power Supply	V_H = 5V				
	Rejection Ratio @ V_{CC}	and ΔV_{CC} = ±200 mV			4	
	@ V_{EE}	V_L = 0V ΔV_{EE} = ±200 mV			4	%

AC Electrical Characteristics

V_{CC} = 10V ±3%, V_{EE} = -5.2V ±5%, T_A = 25°C (still air) and the load is a 50Ω transmission line with 2.0 ns one-way delay, unless otherwise specified. The transmission line is back-terminated in 50Ω (±5%) using both internal and external termination resistance. The measurement probe is a high impedance FET probe with capacitance no greater than 3 pF and resistance no smaller than 10 kΩ.

Symbol	Parameters	Test Conditions	Min.	Typ.	Max.	Units
SLR	Slew Rate	$V_H - V_L$ = 5V; Measured between 20% and 80% points. With probe only as load	3.0	3.5		V/ns
		With probe and transmission line	2.7	3.2		V/ns
+SRC	Positive SLR Control + SRC					
	Control Voltage Range	V_H = +5V, V_L = 0V	-2.0		+2.0	V
	Slew Rate Change		0.5		+3.5	V/ns
–SRC	Negative SLR Control –SRC					
	Control Voltage Range	V_H = +5V, V_L= 0V	-2.0		+2.0	V
	Slew Rate Change		0.5		+3.5	V/ns
t_R,	Rise Time, and	C_L = 5.0 pF				
t_F	Fall Time	V_A = 0.8V (20% to 80%)		0.5	0.8	ns
		V_A = 3V (10% to 90%)		1.0	1.4	ns
		V_A = 5V (10% to 90%)		1.4	1.8	ns

AC Electrical Characteristics (continued)

Symbol	Parameters	Test Conditions	Min.	Typ.	Max.	Units
f	Toggle Rate	Amplitude = 0.8 Vp-p	500	550		MHz
	(Probe only)	Amplitude = 3.0 Vp-p	275	300		MHz
		Amplitude = 5.0 Vp-p	200	220		MHz
t_{PHL}	High to Low Propagation Delay	f = 10 MHz; V_{OH} = +0.4V;				
		V_{OL} = -0.4V		1.7	2.0	ns
Δt_P	Propagation Delay Match	$\lvert t_{PLH} - t_{PHL} \rvert$		30	100	ps
t_PTC	Propagation Delay Temperature Coefficient			2		ps/°C
tPW_{min}	Minimum Pulse Width	V_H - V_L - 2.0V; pulsewidth at which amplitude drops by 50 mV, measured between 50% points. C_L = 5.0 pF		1.1		ns
Δt_PPW	Propagation Delay Variation with Pulse Width	2 ns < PW < 98 ns; f = 10 MHz; V_{OH} = +0.4V; V_{OL} = -0.4V		40	150	ps
t_{PS}	Preshoot	0.5V < V_A < 5.0V		15mV + 3% of V_A		ns
t_{OS}	Overshoot	0.5V < V_A < 5.0V		50mV + 4% of V_A		ns
t_S	Output Settling Time	V_A = 5V;				
		To within 3% of V_A		5.0		ns
		To within 1% of V_A		12.0		ns
t_{PHZ}	Propagation Delay from Logic High to Inhibit Mode	V_{OH} = 1V; V_{OL} = -1V Load = 100Ω to 2.5V; Propagation delay is measured to the point at which voltage has changed by 200 mV.		1.5	2.0	ns
t_{PLZ}	Propagation Delay from Logic Low to Inhibit Mode			2.0	2.5	ns
t_{PZH}	Propagation Delay from Inhibit Mode from Logic High			2.2	2.5	ns
t_{PZL}	Propagation Delay from Inhibit Mode to Logic Low			2.2	2.5	ns
C_Z	Output Capacitance in Inhibit Mode			3.0		pf

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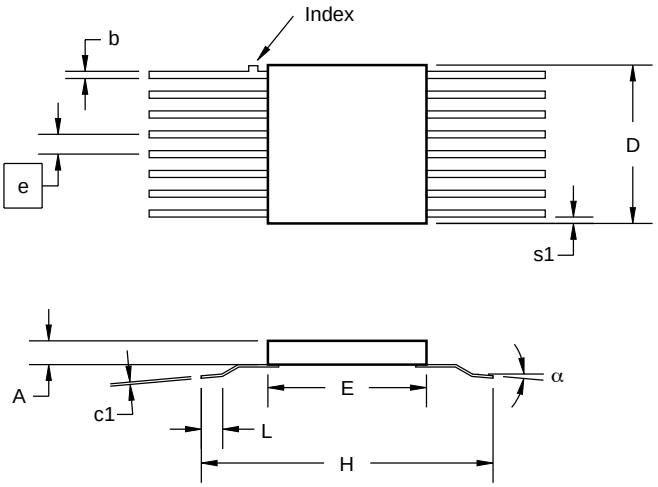
Mechanical Dimensions

16-Lead Hybrid Flatpack

Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.072	.088	1.83	2.24	
b	.013	.017	0.33	0.43	
c1	.007	.010	0.18	.15	
D/E	.442	.458	11.23	11.63	
e	.050 BSC		1.27 BSC		
H	.675	.685	17.15	17.40	
L	.050	.065	1.40	1.65	
s1	.005	-	.13	-	
α	0°	5°	0°	5°	

Notes:

1. All dimensions and tolerances conform to ANSI Y14.5M-1982.
2. Gold plate 80 μ" min. nickel over 80 μ" min. nickel.
3. Leads 1 and 9 connect to ground, seal ring, and heat sink pad.



Ordering Information

Part Number	Package	Operating Temperature Range
RC7316TEL	EL	0°C to +70°C

Notes:
TEL = 16 Lead Hybrid Flatpack, 50Ω termination (AD1322 pinout)